EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ali M. Imam on September 11, 2009.

In the claims, amend claim 9 and cancel claim 10.

9. (Currently Amended) An SPDT (single-pole double-throw) switch for controlling propagation of a high frequency signal between an input terminal and two output terminals, said SPDT switch employing: a plurality of field-effect transistor (FET) switches, each of said plurality of FET switches is connected in parallel with each other, and each of said plurality of FET switches having a field-effect transistor whose drain and source are directly connected in parallel with an inductor; and wherein the input of said plurality of parallel FET switches is directly connected to the input terminal of said SPDT switch and the output of said plurality of parallel FET switches is directly connected to a first output terminal of said [SPST] SPDT switch[.] ; a single field-effect transistor (FET) switch having an inductor directly connected in parallel with a series circuit, the series circuit consisting of a capacitor connected in series with a drain or source of a field-effect transistor; and wherein the input of said single FET switch is directly connected to a second output terminal of said SPDT switch and the output of said single FET switch is directly connected to ground.

10. (Canceled)

Allowable Subject Matter

Claims 1, 4 – 9, 11 and 12 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach or suggest the limitations of the claims.

Nakahara and Matsunaga shows nearly identical SPST (single pole single throw) switches comprising a plurality of field-effect transistor (FET) switches connected in parallel (e.g. each FET shunt connected to each respective transmission line/s branch) and each of said plurality of FET switches having a field-effect transistor whose drain and source are directly connected in parallel with an inductor but does not show where each of the plurality of FET switches are connected in parallel with each other; connecting an inductor in parallel with a series circuit, the series circuit consisting of a capacitor connected in series with a drain or source of FET; or comprising an MPMT (multi-pole multi throw) switch.

Wallace shows a MPMT switch comprising a plurality of input terminals and a plurality of output terminals but does show the input of said plurality of parallel FET switches is directly connected to an input terminal of said MPMT switch and the output of said plurality of parallel FET switches is directly connected to an output terminal of the MPMT switch (where capacitors intervene in the input and output connections of the FET switches); or where each of said FET switches having an inductor directly connected in parallel with a series circuit, the series circuit consisting of a capacitor

connected in series with a drain or source of a field-effect transistor and where the FET switches having their second terminals connected with each other.

Newly cited prior art of Hieda shows a SPDT switch (Fig. 11) comprising a plurality of FET switches having a field-effect transistor whose drain and source are connected in parallel with each other (2b, 2c thru 2a) having a drain and source directly connected in parallel with an inductor but does not show a SPST switch; and MPMT switch; or an SPDT switch comprising connecting an inductor in parallel with a series circuit, the series circuit consisting of a capacitor connected in series with a drain or source of FET; or comprising an MPMT (multi-pole multi throw) switch nor would it have been obvious to combine the prior art of record thus the claims are allowable.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hieda shows a phase shifter switch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEAN O. TAKAOKA whose telephone number is (571)272-1772. The examiner can normally be reached on 9:00a - 5:30p Mon - Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dean O Takaoka/
Primary Examiner, Art Unit 2817